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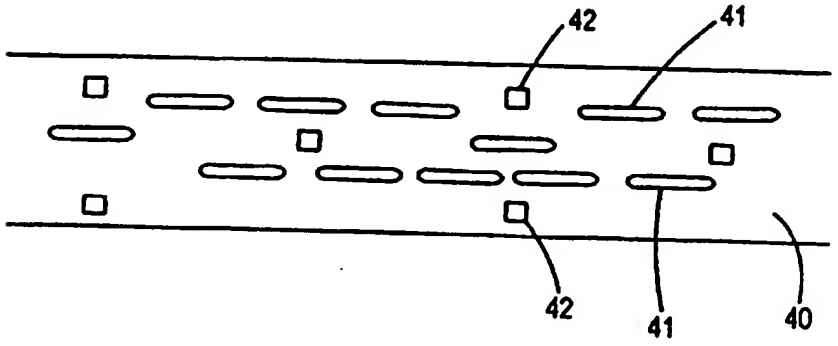

(57) Abstract

The electromigration lifetime of a metal interconnection line is increased by adjusting the length of the interconnection line or providing longitudinally spaced apart holes or vias to optimize the backflow potential capacity of the metal interconnection line. In addition, elongated slots are formed through the metal interconnection line so that the total width of metal across the interconnection line is selected for optimum electromigration lifetime in accordance with the Bamboo Effect for that metal.

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ENHANCED ELECTROMIGRATION LIFETIME OF METAL INTERCONNECTION LINES

Technical Field

The present invention relates to a semiconductor device containing an interconnection line, and to a method of manufacturing the semiconductor device, wherein the lifetime of the interconnection line is maximize with respect to electromigration failure.

Background Art

Conventional semiconductor devices typically comprise a semiconductor substrate, a plurality of insulating and conductive levels formed thereon having a conductive interconnection pattern comprising features and spacings, such as a plurality of spaced apart conductive lines, and several types of conductive interconnection lines, such as bus lines, power supply lines and clock lines, having a width greater than the width of the minimum width conductive lines according to the design rule of the semiconductor device. Increasing demands for density and performance associated with ultra-large scale integration semiconductor wiring require responsive changes in interconnection technology which is considered one of the most demanding aspects of ultra-high scale integration technology. High density demands for ultra-large scale integration semiconductor wiring require planarized layers with minimal design features and spacings, including spacing between conductive lines.

A limitation on the lifetime and reliability of conventional semiconductor devices attributed to conductive interconnection lines is due to electromigration. The phenomenon of electromigration involves the flow of electrons causing the migration of atoms, thereby generating voids and hillocks. The formation of voids creates an opening in a conductive interconnection line, thereby decreasing the performance of the interconnection line. The formation of voids generates areas of increased resistance which undesirably reduce the speed of a semiconductor device. Thus, the electromigration phenomenon constitutes a limitation on the lifetime of a conductive interconnection line as well as the performance of the semiconductor device.

Electromigration in a metal interconnection line can be characterized by the movement of ions induced by a high electrical current density. As the miniaturization of the feature sizes of semiconductor devices increases, the current density also increases and, hence, electromigration induced metallization failures increase. Current metallization failures resulting from electromigration exceed about 30% of the total of metallization failures.

Prior attempts to restrain electromigration involve the use of overcoating, alloying, or multilevel metallization, which approaches do not directly address the electromigration phenomenon. In co-pending U.S. Patent Application Serial No. 08/476,512 (our docket no. 1033-106 filed on June 7, 1995), an approach is disclosed to enhance the electromigration lifetime of a metal interconnection line by optimizing the width of the metal interconnection line consistent with the minimum time for 50% failure by electromigration according to the Bamboo Effect for the metal. The disclosed technique comprises the formation of one or more slots through the metal interconnection line, wherein the number, length and

width of each slot is determined by the Bamboo Effect for that metal so that the width of actual metal across the interconnection line, between the slots, is less than that which corresponds to the minimum time for 50% failure by electromigration according to the Bamboo Effect for that metal. The entire disclosure of copending U.S. Patent Application Serial No. 08/476,512 (our Docket No. 1033-106 filed on June 7, 1995), is incorporated herein by reference.

In a study of the kinetics of electromigration in the 1970's, it was reported that electromigration induced metallic ion accumulation generates a chemical potential gradient which is capable of counteracting or driving the ions in the opposite direction caused by electromigration. This phenomenon is characterized as the Backflow Effect. See Blech, "Electromigration in thin aluminum films on titanium nitride," Journal of Applied Physics, Vol. 47, No. 4, April 1976, pp. 1203-1208.

A subsequent research study on electromigration and the Backflow Effect is reported by Li et al., "Increase in Electromigration Resistance by Enhancing Backflow Effect," IEEE/RPS, 1992, pp. 211-216. Li et al. refer to the work of Dr. Blech and his study of the kinetics of electromigration and the Backflow Effect which was characterized as an inverse electromigration effect which can be employed to offset a certain amount of electromigration induced ion flow. The work reported by Li et al. is directed to enhancing the Backflow Effect and, hence, decreasing electromigration.

In copending U.S. Patent Application Serial No. __ _____ (our Docket No. 1033-116), an approach is disclosed to enhance the electromigration lifetime of a metal interconnection line by optimizing the length, providing one or more strategically longitudinally spaced openings or adjusting the distance

between the points at which the metal interconnection line is in electrical contact with conductive vias, so that the length, distance between the openings or distance between the ends of the interconnection line and an opening, or the longitudinal distance between the conductive vias, is less than the length corresponding to the minimum Backflow Potential Capacity of the metal interconnection line. The entire disclosure of copending U.S. Patent Application Serial No. _____ (our Docket No. 1033-116 filed on August 4, 1995), is incorporated herein in its entirety by reference.

The requirement for long electromigration lifetime remains of critical importance for an interconnection system, particularly an interconnection system in semiconductor devices comprising conductive patterns having submicron features and spacings such as conductive patterns having features greater than about three times the minimum allowed feature for a given design rule involving high electrical current density. Thus, there remains a need in the semiconductor art for increasing the electromigration lifetime of an interconnection line.

Disclosure of the Invention

An object of the present invention is a highly integrated semiconductor device containing an interconnection structure having an enhanced electromigration lifetime.

Another object is an improved method of manufacturing a semiconductor device having a metal interconnection line with an enhanced electromigration lifetime.

Additional objects, advantages and other features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from

practice of the invention. The objects and advantages of the invention may be realized and obtained as particularly pointed out in the appended claims.

According to the present invention, the foregoing and other objects are achieved in part by a semiconductor device comprising: a conductive pattern having features; an insulating layer formed on the conductive pattern; and a metal interconnection line formed on the insulating layer; wherein the metal interconnection line has a length less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line; the metal interconnection line comprise one or more slots through the metal interconnection line to the insulating layer; each slot has a length greater than its width; each slot has a maximum width less than the minimum spacing between the conductive lines; and the minimum width of each slot is equal to the limit of etching or photolithography technology.

Another aspect of the present invention is a semiconductor device comprising: a conductive pattern having features; a first insulating layer formed on the conductive pattern; a first metal interconnection line formed on the first insulating layer; a second insulating layer formed on the first metal interconnection line; and at least two longitudinally spaced apart first conductive vias formed through the second insulating layer in electrical contact with the first metal interconnection line at first contact points separated by a first longitudinal distance which is less than the length corresponding to the minimum Backflow Potential Capacity for the first metal interconnection line; wherein: the metal interconnection line comprise one or more slots through the metal interconnection line to the insulating layer; each slot has a length greater than its width; each slot has a maximum width less than the minimum spacing between the conductive lines; and the minimum

width of each slot is equal to the limit of etching or photolithography technology.

A further aspect of the present invention is a semiconductor device comprising: a conductive pattern having features; an insulating layer formed on the conductive pattern; a metal interconnection line formed on the insulating layer having at least two longitudinally spaced apart openings; wherein the length of the metal interconnection line is greater than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line occurs; the longitudinal distance between the two openings is less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line; the metal interconnection line comprise one or more slots through the metal interconnection line to the insulating layer; each slot has a length greater than its width; each slot has a maximum width less than the minimum spacing between the conductive lines; and the minimum width of each slot is equal to the limit of etching or photolithography technology.

Another aspect of the present invention is a semiconductor device comprising a conductive pattern having features; an insulating layer formed on the conductive pattern; a metal interconnection line formed on the insulating layer having an opening therethrough; wherein: the length of the metal interconnection line is greater than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line and the longitudinal distance from each end to the opening is less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line; the metal interconnection line comprise one or more slots through the metal interconnection line to the insulating layer; each slot has a length greater than its width; each slot has a

maximum width less than the minimum spacing between the conductive lines; and the minimum width of each slot is equal to the limit of etching or photolithography technology.

A further aspect of the present invention is a method of manufacturing a semiconductor device which method comprises: forming a first insulating layer; forming a conductive pattern comprising a plurality of spaced apart conductive lines; forming a second insulating layer on the conductive pattern; forming a metal interconnection line on the second insulating layer; forming at least one elongated slot through the interconnection line to the second insulating layer; wherein: each slot has a length greater than its width; each slot has a maximum width less than the minimum spacing between the conductive lines; the minimum width of each slot is equal to the limit of etching or photolithography technology; and the length of the metal interconnection line is less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line.

Another aspect of the present invention is a method of making a semiconductor device, which method comprises: forming an insulating layer; forming a conductive pattern comprising a plurality of spaced apart metal conductive lines and a metal interconnection line by a dual damascene process wherein openings are provided in the insulating layer which are subsequently filled in with the metal to simultaneously form the metal conductive lines and metal interconnection line; forming at least one elongated slot through the interconnection line to the insulating layer; wherein: each slot has a length greater than its width; each slot has a maximum width less than the minimum spacing between the conductive lines; the minimum width of each slot is equal to the limit of etching or photolithography technology; and the

length of the metal interconnection line is less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line.

Additional objects and advantages of the present invention will become readily apparent to those skilled in this art from the following detailed description, wherein only the preferred embodiment of the invention is shown and described, simply by way of illustration of the best mode contemplated for carrying out the invention. As will be realized, the invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not as restrictive.

Brief Description of Drawings

Fig. 1 is a typical curve illustrating the Bamboo Effect for a metal.

Fig. 2 is a curve illustrating the Backflow Potential Capacity for an aluminum.

Fig. 3 is a top view of a multilevel interconnection of an embodiment of the present invention.

Fig. 4 depicts an embodiment of the present invention applied to a conductive line.

Description of the Invention

The electromigration lifetime of a metal interconnection line constitutes a significant limitation of the capabilities of conventional semiconductor devices, particularly high density devices. The electromigration failure limitation becomes particularly acute as the integrated semiconductor device becomes increasingly higher in performance (faster operating frequency) due to the corresponding increase in current density which increases the electromigration phenomenon.

The present invention addresses and solves that problem by extending the electromigration lifetime of a metal interconnection line, and improving the performance of the semiconductor device.

In copending U.S. Patent Application Serial No. 08/476,512 (our Docket No. 1033-106 filed on June 7, 1995), the entire disclosure of which is incorporated herein in its entirety by reference, an approach is disclosed to extend the electromigration lifetime of a metal interconnection line by taking advantage of the phenomenon called the "Bamboo Effect," which is related to the microstructural characteristics, particularly grain size, of a particular metal system. In order to implement the Bamboo Effect and enhance the electromigration lifetime of a metal interconnection line, the width of the metal interconnection line is optimized consistent with the minimum time for 50% failure by electromigration according to the Bamboo Effect for the metal. To achieve that objective, one or more slots are formed through the metal interconnection line, wherein the number, length and width of each slot is determined by the Bamboo Effect for the metal so that the width of actual metal across the interconnection line, between the slots, is less than that which corresponds to the minimum time for 50% failure by electromigration according to the Bamboo Effect for that metal. The typical curve shown in Fig. 1 illustrates that T_{50z} is a minimum value at W_m representing the maximum width of the metal line, normally about 2 to about 2-1/2 times the average grain size. The area to the left of or less than the minimum T_{50z}, i.e., to the left of W_m represents an area where the electromigration lifetime can be enhanced due to the "Bamboo Effect" where the line width is equal to the grain size or less than two and one-half times the grain size.

In copending U.S. Patent Application Serial No. __ _____ (our Docket No. 1033-116 filed on August 4, 1995) an approach is disclosed for enhancing the electromigration lifetime of a metal interconnection line by optimizing the effective length of a metal interconnection line so that it is less than the length corresponding to the minimum backflow potential capacity for the metal interconnection line. As reported by Li et al., for a particular metal, i.e., a particular elemental metal or a particular alloy, there exists a Backflow Potential Capacity which depends on a gap distance or length of a stripe of the metal. Such a dependence of the Backflow Potential Capacity on the length is shown in Fig. 2 for aluminum. As disclosed in copending U.S. Patent Application Serial No. _____ (our Docket No. 1033-116), the optimization of the Backflow Potential Capacity is achieved by limiting the length of a metal interconnection line, or providing openings and/or contact points with conductive vias separated by longitudinal distance less than length corresponding to the minimum Backflow Potential Capacity of the metal interconnection line.

In accordance with the present invention, both the Bamboo Effect and the Backflow Effect, particularly the Backflow Potential Capacity, are optimized for a particular species of metal employed in a metal interconnection line in a semiconductor device. Thus, in accordance with the present invention, a metal interconnection line is formed on an insulating layer having a width satisfying the design requirements of a particular integrated circuit, which width is greater than that which would benefit from the Bamboo Effect, the electromigration lifetime of the metal, i.e., W_m, is optimized. This is achieved by initially forming an interconnection line having a width consistent with the design requirements of the integrated circuit, i.e., a

width greater than that which can utilize the Bamboo Effect, i.e., greater than W_m in Fig. 1. However, the electromigration lifetime of such a metal interconnection line is increased by the strategic formation of one or more slots throughout the length of the interconnection line. In addition, the metal interconnection line is designed to have a length less than the length corresponding to the minimum Backflow Potential Capacity for that particular metal interconnection line. The minimum Backflow Potential Capacity must be determined for that particular metal, such as for aluminum as shown in Fig. 2.

In accordance with the present invention, various conductive metals can be employed for the interconnection line, such as aluminum, aluminum alloys, copper, copper alloys, silver, silver alloys, gold, gold alloys, refractory metals, refractory metal compounds and refractory metal alloys. The use of a metal interconnection line in accordance with the present invention can be advantageously applied in semiconductor devices having a conductive pattern comprising features greater than about three times the minimum allowed feature for a given design rule.

As disclosed in copending U.S. Patent Application Serial No. 08/476,512 (our Docket No. 1033-106), the number and dimensions of the slots are strategically chosen to implement the Bamboo Effect and, thereby, enhance the electromigration lifetime of the interconnection line. Specifically, the total initial width of metal across the interconnection line, greater than W_m, is reduced by the formation of slots to a final width at which the electromigration lifetime is enhanced by the Bamboo Effect, i.e., less than W_m in Fig. 1. In one embodiment, the slots are selected to have a maximum width which is less than the minimum spacing between conductive lines. In addition, the minimum width of each

slot is limited by conventional technology, i.e., equal to the limit of etching or photolithography technology.

As also disclosed in copending U.S. Patent Application Serial No. 08/476,512 (our Docket No. 1033-106), the strategic selection and design of the slots is represented by the following formula and is designated the "Slot Design Rule":

$$W = 2 W_0 + S; \quad (1)$$

wherein W represents the width of the interconnection line determined by the design requirements of the particular circuitry; W_0 represents the width of metal across the interconnection line outside of the slots; and S represents the width of the slot which should have a maximum width less than the minimum spacings between conductive lines; and a minimum width limited by the capabilities of etching and photolithography technology.

Advantageously, the length of the slot should not be too long, i.e., less than 10 microns, thereby maintaining the resistance of the interconnection line structure in an acceptable range for circuit operations. Basically, the Slot Design Rule can be applied in systems for submicron or micron design rule for the width of conductive lines and/or interwiring spacing.

As disclosed in copending U.S. Patent Application Serial No. _____ (our Docket No. 1033-116), the Backflow Potential Capacity can be employed to reduce electromigration in metal interconnection lines even though the metal interconnection line has a length greater than the length corresponding to the minimum Backflow Potential Capacity for that metal interconnection line. For example, a metal interconnection line is formed on an insulating layer, which metal interconnection line has a length greater than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line. However, one or more longitudinally spaced apart

openings, preferably longitudinally aligned openings, are formed through the metal interconnection line so that the distance between the ends of the metal interconnection line and an opening, or the distance between two longitudinally spaced apart openings is less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line. The optimum size of the opening depends upon the particular metal and the width of the metal interconnection line, and could easily be determined in a particular situation by one having ordinary skill in the art. The openings in the metal interconnection line can be formed by conventional photolithographic and etching techniques, particularly anisotropic etching, such as reactive ion etching. Damascene techniques can also be employed to form the openings.

The present invention is also applicable to multilevel interconnection patterns. Typically, semiconductor devices comprises a substrate and a plurality of levels with conductive patterns in electrical contact by means of conductive vias and interconnection lines. As disclosed in copending U.S. Patent Application Serial No. _____ (our Docket No. 1033-116), the longitudinal distance between the contact points of conductive vias on the surface of a metal interconnection line is strategically designed so that it is less than the length corresponding to the minimum Backflow Potential Capacity for the particular metal interconnection line.

Thus, in accordance with the present invention, a semiconductor device is formed comprising a conductive pattern and a first insulating layer formed on the conductive pattern. A first metal interconnection line is formed on the first insulating layer and a second insulating layer is formed on the first metal interconnection line. In this embodiment, as in all

embodiments of the present invention, the metal interconnection lines are provided with slots to optimize the Bamboo Effect as disclosed in copending U.S. Patent Application Serial No. 08/476,512 (our Docket No. 1033-106). In addition thereto, the various embodiments of the present invention involve optimization of the effective length of an interconnection line in accordance with Backflow Potential Capacity to further reduce the electromigration phenomenon and, hence, further increase electromigration lifetime. Thus, at least two spaced apart first conductive vias are formed through the second insulating layer in electrical contact with the first metal interconnection line at first longitudinally spaced apart contact points a first longitudinal distance which is less than the length corresponding to the minimum Backflow Potential Capacity for the first metal interconnection line. The length of the first metal interconnection line can, therefore, exceed the length corresponding to the minimum Backflow Potential Capacity for the first metal interconnection line, while optimizing the Backflow Potential Capacity of the metal interconnection line to reduce electromigration failure. As also disclosed in copending U.S. Patent Application Serial No. _____ (our Docket No. 1033-116), the Backflow Potential Capacity is further optimized by employing a material to fill the conductive via different from the metal of the interconnection line. Thus, when employing an aluminum or aluminum alloy metal interconnection line, it is preferred to employ a tungsten plug filling the via or a plug comprising aluminum or aluminum alloy with a barrier layer and/or anti-reflection coating. Typical barrier materials include tungsten, tungsten-titanium, titanium, titanium/titanium nitride, titanium nitride or titanium oxynitride, while typical anti-reflective coatings can comprise titanium nitride or titanium oxynitride.

As further disclosed in copending U.S. Patent Application Serial No. _____ (our Docket No. 1033-116), the Backflow Potential Capacity is utilized to reduce electromigration failure in a plurality of metal interconnection lines on different levels in electrical contact through a via. Thus, the present invention comprises forming a first insulating layer on a conductive pattern, and a first metal interconnection line formed on the first insulating layer. A second insulating layer is formed on the first metal interconnection line with at least two longitudinally spaced apart first conductive vias formed through the second insulating layer in electrical contact with the first metal interconnection line at first longitudinally spaced apart contact points separated by a first longitudinal distance which is less than the length corresponding to the minimum Backflow Potential Capacity for the first metal interconnection line. In addition, slots are provided in the first metal interconnection line, to optimize the Bamboo Effect. A second metal interconnection line is then formed on the second insulating layer. The Backflow Potential Capacity is optimized for the second metal interconnection line in accordance with various aspects of the present invention. For example, the Backflow Potential Capacity is optimized for the second metal interconnection line by confining its length to less than the length corresponding to the minimum Backflow Potential Capacity for the second metal interconnection line. In addition, slots are provided in the second metal interconnection line to optimize the Bamboo Effect. As disclosed in copending U.S. Patent Application Serial No. 08/476,512 (our Docket No. 1033-106), the Bamboo Effect for the second metal interconnection line can also be optimized by providing at least one opening therethrough. The openings for optimizing the Backflow Potential Capacity are not

governed by the numerical and dimensional restrictions designed to optimize the Bamboo Effect. Rather, these openings, as disclosed in copending U.S. Patent Application Serial No. _____ (our Docket No. 1033-116) are designed to provide discontinuities for optimizing the Backflow Potential Capacity and are preferably longitudinally aligned. Thus, openings provided through the second metal interconnection line are strategically placed so that the longitudinal distance between each end of the second metal interconnection line and an opening, or the longitudinal distance between two openings, is less than the length corresponding to the minimum Backflow Potential Capacity for the second metal interconnection line.

The Backflow Potential Capacity is utilized to reduce electromigration failure in multilevel metal interconnection lines by forming a third insulating layer on the second metal interconnection line in electrical contact. At least one second conductive via is formed through the third insulating layer in electrical contact with the second metal interconnection line at a third contact point longitudinally spaced from the second contact point on the second metal interconnection line by a second longitudinal distance which is less than the length corresponding to the minimum Backflow Potential Capacity for the second metal interconnection line.

As disclosed in copending U.S. Patent Application Serial No. _____ (our Docket No. 1033-116), dimensional considerations are applicable for optimizing the Backflow Potential Capacity of multilevel metal interconnection lines. Thus, the situations where the width of the first and second metal interconnection lines are substantially the same, the optimum length of the second metal interconnection line L_2 and the optimum second longitudinal distance D_2 are represented by the following formulas:

$$L_2 = D_1 \left(\frac{T_2}{T_1}\right); \text{ wherein} \qquad (2)$$

wherein D_1 is the first longitudinal distance, T_2 is the thickness of the second metal interconnection line and T_1 is the thickness of the first metal interconnection line; and

$$D_2 = D_1 \left(\frac{T_2}{T_1}\right); \text{ wherein} \qquad (3)$$

D_1, D_2 and T_1 are as previously defined.

If the width of the first and second metal interconnection lines are that substantially equal, the optimum longitudinal length L_2 and distance D_2 are represented by the following formulas:

$$L_2 = D_1 \left(\frac{T_2}{T_1}\right) \left(\frac{W_2}{W_1}\right); \text{ wherein,} \qquad (4)$$

D_1, T_1 and T_2 are as previously defined, W_2 is the width of the second metal interconnection line and W_1 is the width of the first metal interconnection line; and

$$D_2 = D_1 \left(\frac{T_2}{T_1}\right)\left(\frac{W_2}{W_1}\right); \text{ wherein} \qquad (5)$$

D_1, D_2, T_2, T_1, W_2 and W_1 are as previously defined.

As shown in Fig. 3, first metal interconnection line 30 is in electrical contact with vias 32A and 32B at contact points longitudinally separated by distance D_1. Second metal interconnection line 31, which has a width greater than that of first metal interconnection line 30, is in electrical contact with vias 32B and 32C at contact points longitudinally separated by a distance of D_2. Metal interconnection lines 30 and 31 are additional provided with slots 33. The distances D_1 and D_2 are selected in accordance with formula (5) whereby the Backflow Effect is optimized; while the number and dimension of the slots are governed in accordance with formula (1) wherein the Bamboo Effect is optimized.

An embodiment of the present invention as applied to a conductive line is depicted in Fig. 4, wherein reference numeral 40 denotes a conductive line which has been provided with slots and openings in accordance with the present invention. As shown in Fig. 4, conductive line 40 is provided with a plurality of elongated slots 41 in order to optimize the width of conductive line 40 consistent with the Bamboo Effect for the metal of the conductive line 40. In addition, conductive line 40 is provided with a plurality of openings 42 designed to optimize the Backflow Potential Capacity for the metal comprising conductive line 40.

The present invention is applicable of all types of semiconductor devices wherein metal interconnection lines are provided, such as bus lines, power supply lines and/or clock lines. In carrying out the present

invention, conventional methods of forming conductive patterns comprising features and spacings, such as a plurality of spaced apart conductive lines, and metal interconnection lines can be employed, such as conventional photolithographic techniques, etching techniques and damascene techniques. The present invention is applicable to semiconductor devices comprising interconnection patterns having a wide range of dimensions, including submicron dimensions, which conductive patterns are formed in a conventional manner, as by conventional etch back techniques or single and/or dual damascene techniques.

Typically, a first insulating layer is deposited and a conductive pattern formed. The conductive pattern can be formed by conventional etch back techniques involving the deposition of a metal layer and etching to form a conductive pattern comprising a plurality of spaced apart conductive lines. The conductive pattern can also be formed by a damascene technique in which openings are formed in the insulating layer and metal deposited in the openings to form the conductive pattern. Subsequently, a second insulating layer is deposited and a metal interconnection line is formed on the second insulating layer. The conductive pattern and interconnection line can be formed by a dual damascene technique in which the conductive pattern and metal interconnection line are deposited by a single metal deposition process.

Damascene is an art which has been employed for centuries in the fabrication of jewelry, and has recently been adapted for application in the semiconductor industry. Damascene basically involves the formation of a trench which is filled with a metal. Thus, damascene differs from the traditional etch back techniques of providing an interconnection structure by forming a pattern of trenches in a dielectric layer, which trenches are filled in with metal to form the conductive pattern

followed by planarization vis-à-vis the traditional etch back technique of depositing a metal layer, forming a conductive pattern with interwiring spacings, and filling in the interwiring spacings with dielectric material. Single and dual damascene techniques have also been employed to form openings in a dielectric layer which are subsequently filled with metal. The application of damascene techniques to the manufacture of semiconductor devices is disclosed in Joshi, "A New Damascene Structure for Submicrometer Interconnect Wiring," IEEE Electron Letters, Vol. 14, No. 3, March 1993, pp. 129-132; Kaanta et al., "Dual Damascene: A ULSI Wiring Technology," June 11-12, 1991, VMIC Conference, IEEE, pp. 144-152; Kenney et al., "A Buried-Plate Trench Cell for a 64-Mb DRAM," 1992 Symposium on VLSI Technology Digest of Technical Papers, IEEE, pp. 14-15; U.S. Patent No. 5,262,354; and U.S. Patent No. 5,093,279.

In forming interconnection lines in accordance with the present invention employing a damascene technique, portions of the dielectric layer in the trench are not etched. Af ther trench is filled in with metal, the unetched portions of the dielectric layer form slots in the interconnection layer for optimizing the Bamboo Effect and openings for optimizing the Backflow Potential Capacity. After formation of the wiring pattern, planarization is effected as by chemical-mechanical polishing.

In carrying out the present invention, the interconnection line can be formed of any metal typically employed for forming an interconnection line, such as aluminum, aluminum alloys, copper, copper alloys, gold, gold alloys, silver, silver alloys, refractory metals, refractory metal alloys, and refractory metal compounds. A conventional adhesion/barrier layer can also be mployed, such as titanium, titanium-tungsten, titanium nitride or titanium oxynitride. The metal

interconnection line of the present invention can be formed by any technique conventionally employed in the manufacture of semiconductor devices. For example, the method interconnection line can be formed by conventional metallization techniques, such as various types of chemical vapor deposition (CVD) processes, including low pressure chemical vapor deposition (LPCVD), and plasma enhanced chemical vapor deposition (PECVD). Normally, when high melting metal points such as tungsten are deposited, CVD techniques are employed. Low melting point metals, such as aluminum and aluminum-base alloys, including aluminum-copper alloys, can be deposited by melting, sputtering or physical vapor deposition (PVD).

The present invention is also applicable to the manufacture of semiconductor devices comprising a plurality of conductive patterns formed on different levels, including conductive patterns formed by etch back techniques and/or damascene and dual damascene techniques. In a preferred embodiment, such semiconductor devices comprising a plurality of conductive patterns on different levels also comprise a plurality of metal interconnection lines, having a length less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line, or having a length adjusted, as by openings or vias, so that the distance between the openings or vias is less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line, thereby reducing electromigration and enhancing the electromigration lifetime of the metal interconnection line. In addition, the metal interconnection lines are provided with the slots, wherein each slot has a length greater than its width, each slot has a maximum width less than the minimum spacing between conductive lines, and the minimum width of each slot is equal to the limit

of conventional etching of photolithographic techniques thereby optimizing the Bamboo Effect.

The semiconductor devices to which the claimed invention is directed generally comprise insulating layers formed of insulating materials conventionally employed in the manufacture of semiconductor devices, such as silicon dioxide, including silicon dioxide formed by thermal oxidation, vapor deposition and/or derived from deposited tetraethyl orthosilicate (TEOS), silicon nitride, silicon oxynitrides and/or low dielectric constant materials. Insulating material can be deposited in a conventional manner, as by CVD or thermal enhanced CVD and spin-on techniques. The various embodiments of the present invention involve a conventional semiconductor substrate, such as monocrystalline silicon.

Thus, in accordance with the present invention, the length of a metal interconnection line is advantageously selected in accordance with the design requirements for a particular integrated circuit, while advantageously maximizing the electromigration lifetime by optimizing the Backflow Potential Capacity for the particular metal interconnection line, as by selecting an appropriate line length, providing one or more strategically longitudinally spaced holes or adjusting the distance between the points at which the metal interconnection line is in electrical contact with conductive vias, so that the longitudinal distance between the holes or vias is less than the length corresponding to the minimum Backflow Potential Capacity of the metal interconnection line. In addition, the width of the metal interconnection line is advantageously selected in accordance with the design requirements for a particular integrated circuit, while advantageously maximizing the electromigration lifetime by providing slots, the number and configuration of which are selected to provide a width of actual metal across the interconnection line,

between the slots, less than that which corresponds to the minimum time for 50% failure by electromigration according to the Bamboo Effect for that metal.

Only the preferred embodiment of the invention and an example of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein.

CLAIMS

1. A semiconductor device comprising:

a conductive pattern having features;

an insulating layer formed on the conductive pattern; and

a metal interconnection line formed on the insulating layer; wherein:

the metal interconnection line has a length less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line;

the metal interconnection line comprises one or more slots through the metal interconnection line to the insulating layer;

each slot has a length greater than its width;

each slot has a maximum width less than the minimum spacing between the conductive lines; and

the minimum width of each slot is equal to the limit of etching or photolithography technology.

2. The semiconductor device according to claim 1, wherein the length of each slot is less than about 10 microns.

3. The semiconductor device according to claim 1, wherein the metal is selected from the group consisting of aluminum, aluminum alloys, copper, copper alloys, silver, silver alloys, gold, gold alloys, refractory metals, refractory metal compounds and refractory metal alloys.

4. The semiconductor device according to claim 3, wherein the metal comprises tungsten or a tungsten alloy.

5. The semiconductor device according to claim 3, wherein the metal comprises aluminum or an aluminum alloy.

6. The semiconductor device according to claim 1, wherein the conductive pattern comprises features greater than about three times the minimum allowed feature for a given design rule.

7. The semiconductor device according to claim 1, wherein the conductive pattern comprises a plurality of spaced apart conductive lines, and wherein the width of the interconnection line is at least twice the width of a minimum conductive line in accordance with the design rule.

8. The semiconductor device according to claim 1, wherein the number and width of each slot are selected to provide a width of actual metal across the interconnection line, between the slots, which is less than that corresponding to the minimum time for 50% failure by electromigration according to the Bamboo Effect for that metal.

9. A semiconductor device comprising:

a conductive pattern having features;

a first insulating layer formed on the conductive pattern;

a first metal interconnection line formed on the first insulating layer;

a second insulating layer formed on the first metal interconnection line; and

at least two longitudinally spaced apart first conductive vias formed through the second insulating layer in electrical contact with the first metal interconnection line at first contact points separated by a first longitudinal distance which is less than the length corresponding to the minimum Backflow Potential Capacity for the first metal interconnection line; wherein:

the metal interconnection line comprises one or more slots through the metal interconnection line to the insulating layer;

each slot has a length greater than its width;

each slot has a maximum width less than the minimum spacing between the conductive lines; and

the minimum width of each slot is equal to the limit of etching or photolithography technology.

10. The semiconductor device according to claim 9, wherein the length of each slot is less than about 10 microns.

11. The semiconductor device according to claim 9, wherein the metal interconnection line comprise a metal selected from the group consisting of aluminum, aluminum alloys, copper, copper alloys, silver, silver alloys, gold, gold alloys, refractory metals, refractory metal compounds and refractory metal alloys.

12. The semiconductor device according to claim 11, wherein the metal is aluminum or an aluminum alloy.

13. The semiconductor device according to claim 9, wherein the first conductive vias are filled with a metal.

14. The semiconductor device according to claim 12, wherein the first conductive vias are filled with aluminum or an aluminum alloy, and a barrier layer is interposed between the aluminum or aluminum alloy and the first metal interconnection line.

15. The semiconductor device according to claim 14, wherein the barrier layer comprises titanium, titanium-tungsten or titanium nitride.

16. The semiconductor device according to claim 12, wherein the first conductive vias are filled with aluminum or an aluminum alloy, and an anti-reflection coating is provided on the aluminum or aluminum alloy.

17. The semiconductor device according to claim 16, wherein the anti-reflection coating comprises titanium or a titanium oxynitride.

18. The semiconductor device according to claim 11, wherein the metal is tungsten.

19. The semiconductor device according to claim 9, wherein the length of the first metal interconnection line is greater than the length corresponding to the minimum Backflow Potential Capacity for the first metal interconnection line.

20. The semiconductor device according to claim 9, further comprising a second metal interconnection line formed on the second insulating layer and in electrical

contact with one of the first conductive vias at a second contact point.

21. The semiconductor device according to claim 20, wherein the second metal interconnection line has a length less than the length corresponding to the minimum Backflow Potential Capacity for the second metal interconnection line.

22. The semiconductor device according to claim 20, further comprising:

a third insulating layer formed on the second metal interconnection line; and

at least one second conductive via formed through the third insulating layer in electrical contact with the second metal interconnection line at a third contact point longitudinally spaced apart from the second contact point on the second metal interconnection line by a second longitudinal distance which is less than the length corresponding to the minimum Backflow Potential Capacity for the second metal interconnection line.

23. The semiconductor device according to claim 20, wherein the width of the first metal interconnection line is essentially the same as the width of the second metal interconnection line.

24. The semiconductor device according to claim 23, wherein the length of the second metal interconnection line (L_2) is represented by the formula:

$$L_2 = D_1 \left(\frac{T_2}{T_1}\right); \text{ wherein}$$

D_1 is the first longitudinal distance; T_2 is the thickness of the second metal interconnection line, and

T_1 is the thickness of the first metal interconnection line.

25. The semiconductor device according to claim 22, wherein the width of the first metal interconnection line is essentially the same as the width of the second metal interconnection line.

26. The semiconductor device according to claim 25, wherein the second longitudinal distance D_2 is represented by the formula:

$$D_2 = D_1 \left(\frac{T_2}{T_1}\right); \text{ wherein}$$

D_1 is the first longitudinal distance, T_2 is the thickness of the second metal interconnection line and T_1 is the thickness of the first metal interconnection line.

27. The semiconductor device according to claim 20, wherein the width of the first metal interconnection line is not substantially equal to the width of the second metal interconnection line.

28. The semiconductor device according to claim 27, wherein the length of the second metal interconnection line (L_2) is represented by the formula:

$$L_2 = D_1 \left(\frac{T_2}{T_1}\right) \left(\frac{W_2}{W_1}\right); \text{ wherein}$$

D_1 is the first longitudinal distance, T_2 is the thickness of the second metal interconnection line; T_1 is the thickness of the first metal interconnection line; W_2 is the width of the second metal interconnection line;

and W_1 is the width of the first metal interconnection line.

29. The semiconductor device according to claim 22, wherein the width of the first metal interconnection line is not substantially equal to the width of the second metal interconnection line.

30. The semiconductor device according to claim 28, wherein the second longitudinal distance (D_2) is represented by the formula:

$$D_2 = D_1 \left(\frac{T_2}{T_1}\right) \left(\frac{W_2}{W_1}\right); \text{ wherein}$$

D_1 is the first longitudinal distance, T_2 is the thickness of the second metal interconnection line; T_1 is the thickness of the first metal interconnection line; W_2 is the width of the second metal interconnection line; and W_1 is the width of the first metal interconnection line.

31. The semiconductor device according to claim 22, wherein the length of the second metal interconnection line is greater than the length corresponding to the minimum Backflow Potential Capacity for the second metal interconnection line.

32. The semiconductor device according to claim 20, wherein the second metal interconnection layer has a length greater than the length corresponding to the minimum Backflow Potential Capacity for the second metal interconnection line; and

the second metal interconnection layer comprises at least two longitudinally spaced apart openings extending therethrough; wherein the longitudinal distance between

the two openings is less than the length corresponding to the minimum Backflow Potential Capacity for the second metal interconnection line.

33. The semiconductor device according to claim 32, wherein the openings are longitudinally aligned.

34. The semiconductor device according to claim 9, wherein the conductive pattern comprises features greater than about three times the minimum allowed feature for a given design rule.

35. The semiconductor device according to claim 9, wherein the conductive pattern comprises a plurality of spaced apart conductive lines, and wherein the width of the interconnection line is at least twice the width of a minimum conductive line in accordance with the design rule.

36. The semiconductor device according to claim 9, wherein the number and width of each slot are selected to provide a width of actual metal across the interconnection line, between the slots, which is less than that corresponding to the minimum time for 50% failure by electromigration according to the Bamboo Effect for that metal.

37. The semiconductor device according to claim 11, wherein the metal comprises tungsten or a tungsten alloy.

38. A semiconductor device comprising:

a conductive pattern having features;

an insulating layer formed on the conductive pattern;

a metal interconnection line formed on the insulating layer having at least two longitudinally spaced apart openings; wherein:

the length of the metal interconnection line is greater than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line occurs;

the longitudinal distance between the two openings is less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line;

the metal interconnection line comprises one or more slots through the metal interconnection line to the insulating layer;

each slot has a length greater than its width;

each slot has a maximum width less than the minimum spacing between the conductive lines; and

the minimum width of each slot is equal to the limit of etching or photolithography technology.

39. The semiconductor device according to claim 38, wherein the length of each slot is less than about 10 microns.

40. The semiconductor device according to claim 38, wherein the conductive pattern comprises features greater than about three times the minimum allowed feature for a given design rule.

41. The semiconductor device according to claim 38, wherein the openings are longitudinally aligned.

42. The semiconductor device according to claim 38, wherein the conductive pattern comprises a plurality of spaced apart conductive lines, and wherein the width of the interconnection line is at least twice the width of a minimum conductive line in accordance with the design rule.

43. The semiconductor device according to claim 39, wherein the number and width of each slot are selected to provide a width of actual metal across the interconnection line, between the slots, which is less than that corresponding to the minimum time for 50% failure by electromigration according to the Bamboo Effect for that metal.

44. A semiconductor device comprising:

a conductive pattern having features;

an insulating layer formed on the conductive pattern;

a metal interconnection line formed on the insulating layer having an opening therethrough; wherein:

the length of the metal interconnection line is greater than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line and the longitudinal distance from each end to the opening is less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line;

the metal interconnection line comprises one or more slots through the metal interconnection line to the insulating layer;

each slot has a length greater than its width;

each slot has a maximum width less than the minimum spacing between the conductive lines; and

the minimum width of each slot is equal to the limit of etching or photolithography technology.

45. The semiconductor device according to claim 44, wherein the length of each slot is less than about 10 microns.

46. The semiconductor device according to claim 44, wherein the conductive pattern comprises a plurality of spaced apart conductive lines, and wherein the width of the interconnection line is at least twice the width of a minimum conductive line in accordance with the design rule.

47. The semiconductor device according to claim 44, wherein the number and width of each slot are selected to provide a width of actual metal across the interconnection line, between the slots, which is less than that corresponding to the minimum time for 50% failure by electromigration according to the Bamboo Effect for that metal.

48. A method of manufacturing a semiconductor device, which method comprises:

forming a first insulating layer;

forming a conductive pattern comprising a plurality of spaced apart conductive lines;

forming a second insulating layer on the conductive pattern;

forming a metal interconnection line on the second insulating layer;

forming at least one elongated slot through the interconnection line to the s cond insulating layer; wherein:

each slot has a length greater than its width;

each slot has a maximum width less than the minimum spacing between the conductive lines;

the minimum width of each slot is equal to the limit of etching or photolithography technology; and

the length of the metal interconnection line is less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line.

49. The method according to claim 48, wherein the length of each slot is less than about 10 microns.

50. The method according to claim 48, wherein the interconnection line has a width at least twice the width of a conductive line.

51. The method according to claim 48, wherein the number and width of each slot are selected to provide a width of actual metal across the interconnection line, between the slots, which is less than that corresponding to the minimum time for 50% failure by electromigration according to the Bamboo Effect for that metal.

52. The method according to claim 48, wherein the conductive pattern is formed by a damascene process in which trenches are formed in the first insulating layer which are subsequently filled in with metal.

53. A method of manufacturing a semiconductor device, which method comprises:

forming an insulating layer;

forming a conductive pattern comprising a plurality of spaced apart metal conductive lines and a metal interconnection line by a dual damascene process wherein openings are provided in the insulating layer which are subsequently filled in with the metal to simultaneously form the metal conductive lines and metal interconnection line;

forming at least one elongated slot through the interconnection line to the insulating layer; wherein:

each slot has a length greater than its width;

each slot has a maximum width less than the minimum spacing between the conductive lines;

the minimum width of each slot is equal to the limit of etching or photolithography technology; and

the length of the metal interconnection line is less than the length corresponding to the minimum Backflow Potential Capacity for the metal interconnection line.

54. The method according to claim 53, wherein the number and width of each slot are selected to provide a width of actual metal across the interconnection line, between the slots, which is less than that corresponding to the minimum time for 50% failure by electromigration according to the Bamboo Effect for that metal.

55. The method according to claim 54, wherein the interconnection line has a width at least twice the width of a minimum conductive line in accordance with the design rule.

56. The method according to claim 55, further comprising forming a third insulating layer on the first metal interconnection layer; and forming at least two longitudinally spaced apart conductive vias through the second insulating layer in electrical contact with the first metal interconnection line at contact points longitudinally separated by a distance which is less than the length corresponding to the minimum backflow capacity for a first metal interconnection line.

57. The method according to claim 52, wherein the trenches are formed with portions of dielectric material remaining therein, whereby the dielectric portions form the slots.

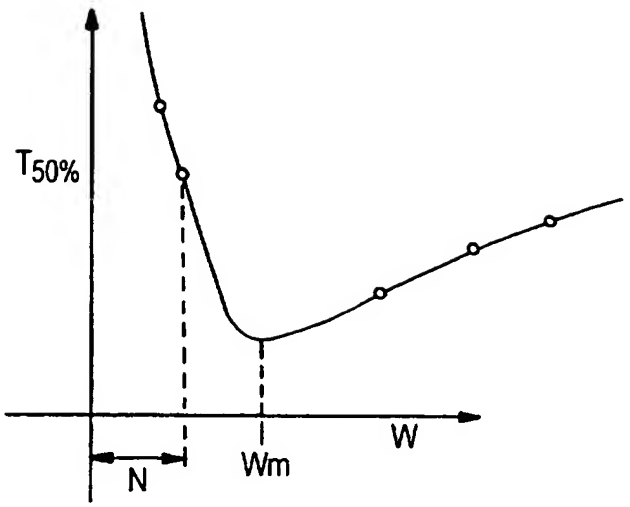
T50%
N
Wm
W

FIG. 1

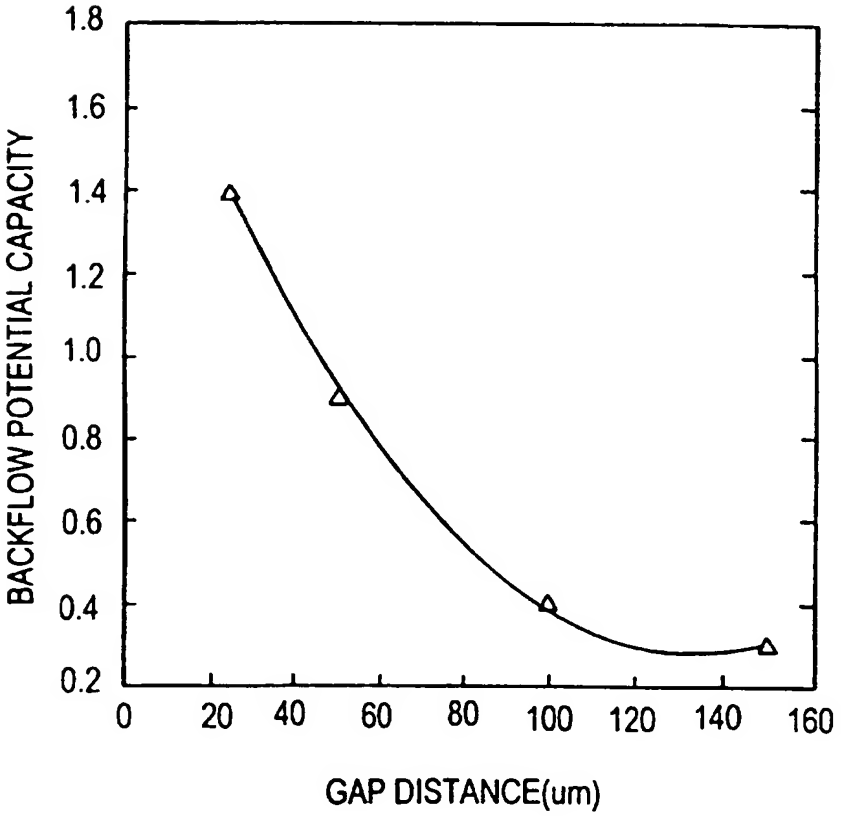
BACKFLOW POTENTIAL CAPACITY
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
20
40
60
80
100
120
140
160
GAP DISTANCE(um)

FIG. 2

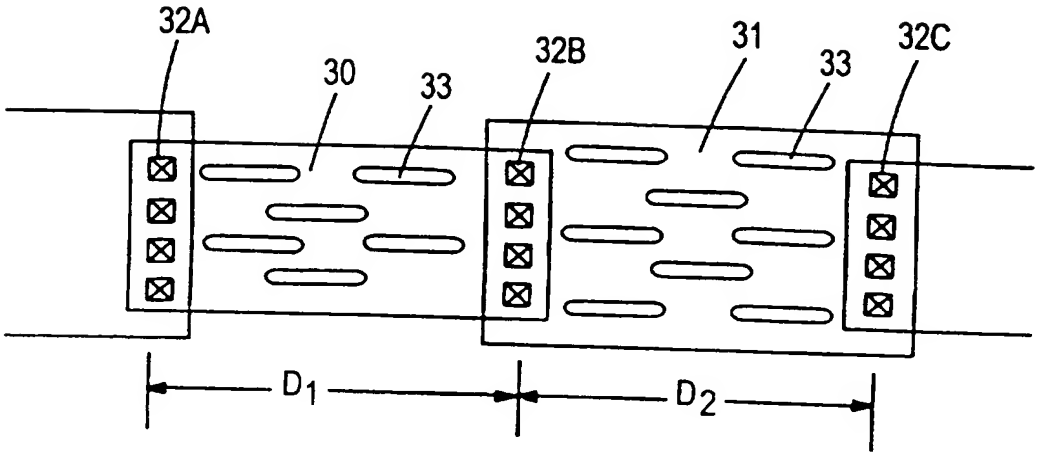

FIG. 3

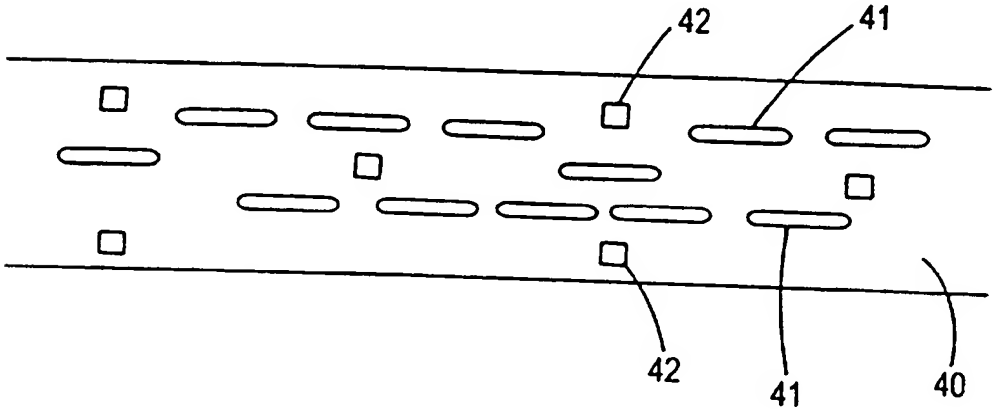

FIG. 4

INTERNATIONAL SEARCH REPORT

Int ional Application No
PCT/US 96/13033

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/532

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	IEEE 30TH ANNUAL PROCEEDINGS RELIABILITY PHYSICS, 31 March 1992 - 2 April 1992, SAN DIEGO, US, pages 211-216, XP000603323 LI ET AL: "Increase in Electromigration resistance by enhancing backflow effect" cited in the application see page 214, left-hand column, line 3-9; figures 6,7 --- -/--	1,3,5,9, 11,12, 38,44, 48,53

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 November 1996	22. 11. 96

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Int. ...nal Application No
PCT/US 96/13033

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A,5 136 361 (WOLLESEN DONALD L ET AL) 4 August 1992 see column 5, line 17 - column 6, line 23; figures 1E,2	1,3-5,9, 11,12, 38,44, 48,53
A	---	13-15, 18,37
Y	US,A,5 382 831 (ATAKOV EUGENIA M ET AL) 17 January 1995 see column 6, line 46 - column 7, line 6; figures 9,11,14,15 see column 11, line 5 - column 12, line 6	1,9,38, 44,48,53
P,Y	--- US,A,5 470 788 (BIERY GLENN A ET AL) 28 November 1995 see column 1, line 36 - column 2, line 23; figure 1	1,3-5, 38,44, 48,53
A	--- 33RD ANNUAL PROCEEDINGS OF 1995 IEEE INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM, 4 - 6 April 1995, LAS VEGAS, USA, pages 365-370, XP000605336 WEI ZHANG ET AL: "An increase in the electromigration reliability of ohmic contacts by enhancing backflow effect" see page 370, left-hand column, paragraph 2; figure 1	1,9,38, 44,48,53
A	--- US,A,5 262 354 (COTE WILLIAM J ET AL) 16 November 1993 cited in the application see claim 1	52
Y	--- PROC. 8TH INTERNATIONAL VLSI MIC CONFERENCE, 11 - 12 June 1991, SANTA CLARA, CA, USA, pages 144-152, XP000601842 C.W. KAANTA ET AL: "Dual Damascene: A ULSI wiring technology" cited in the application see page 145, paragraph 1 - page 146, paragraph 2	53

2

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int onal Application No
PCT/US 96/13033

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-5136361	04-08-92	DE-A-	3382482	30-01-92
		EP-A-	0120918	10-10-84
		JP-T-	59501845	01-11-84
		WO-A-	8401471	12-04-84
US-A-5382831	17-01-95	NONE		
US-A-5470788	28-11-95	JP-A-	7245307	19-09-95
US-A-5262354	16-11-93	CN-A,B	1076547	22-09-93
		EP-A-	0558004	01-09-93
		JP-A-	6084826	25-03-94

CLIPPEDIMAGE= WO009710614A1
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DOCUMENT-IDENTIFIER: WO 9710614 A1
TITLE: ENHANCED ELECTROMIGRATION LIFETIME OF METAL INTERCONNECTION LINES

PUBN-DATE: March 20, 1997

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APPL-NO: US09613033
APPL-DATE: August 8, 1996

PRIORITY-DATA: US52618995A (September 11, 1995)
INT-CL_(IPC): H01L023/532

ABSTRACT:
The electromigration lifetime of a metal interconnection line is increased by adjusting the length of the interconnection line or providing longitudinally spaced apart holes or vias to optimize the backflow potential capacity of the metal interconnection line. In addition, elongated slots are formed through the metal interconnection line so that the total width of metal across the interconnection line is selected for optimum electromigration lifetime in accordance with the Bamboo Effect for that metal.